3 Flip-Flops

Flip-flops and latches are digital memory circuits that can remain in the state in which they were set even after the input signals have been removed. This means that the circuits have a memory function and will hold a value (0 or 1) until the circuit is forced to change state.

A *latch* is a memory device that samples and acts upon its input lines immediately the input lines change. It does not require any external timing signals.

A *flip-flop* is a memory device that samples and acts upon its input lines only when it is told to do so with a special timing signal called the clock. This may be in the form of a level or an edge. A level trigger means that the flip-flop samples its inputs depending upon the voltage level of the trigger input. An edge trigger means that the flip-flop samples its inputs depending on a LOW-to-HIGH transition on the trigger line or a HIGH-to-LOW transistion on a trigger line.

3.1 RS Latches

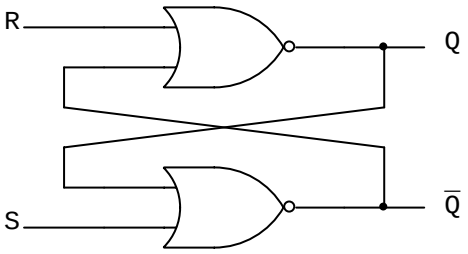
The latch is a logic block that has 2 stable states (0) or (1).

The RS latch can be forced to hold a 1 when the Set line is asserted.

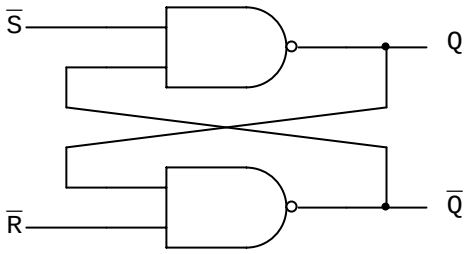
The RS latch can be forced to hold a 0 when the Reset line is asserted.

The RS latch will hold it current value (state) if the Set and Reset lines are not asserted.

The circuit for he RS latch can be seen below.



Cross-coupled NOR RS latch



Cross-coupled NAND RS latch

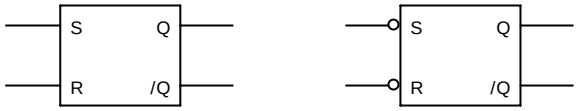
The most noticeable thing about the latch is that it has a feedback path from the output to the inputs. It is this feedback path which enables it to hold a value even when the inputs are not asserted.

There are two types of RS latch. Cross-coupled NOR and cross-coupled NAND.

The NOR type has high active R and S inputs. This means they perform their prescribed action when the lines are high.

The NAND type has low active R and S inputs. This means they perform their prescribed action when the lines are low.

The symbols for the RS latches are shown below:



Active High **Active Low**

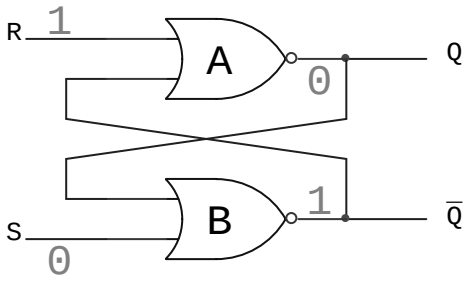
Active High indicates that a high (1) will activate the line.

Active Low indicates that a low (0) will activate the line.

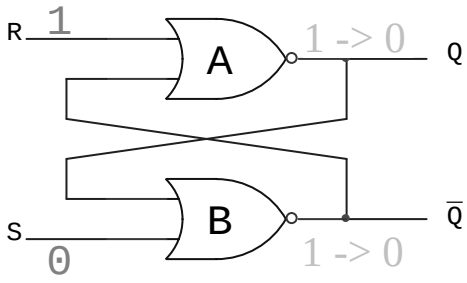
To understand the operation of the RS it is instructive to trace through the logic signals when different values are placed on the R and S lines. Due to the feedback, this may require tracing the lines at least twice until the latch is in a stable state.

For simplicity we will examine the cross-coupled NOR latch since it is high active.

3.1.1 Reset Condition



Q = 0, /Q = 1



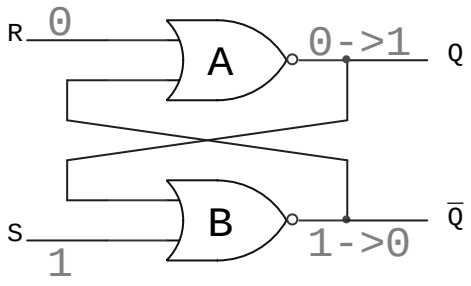
Q = 1, /Q = 0

Analysis:

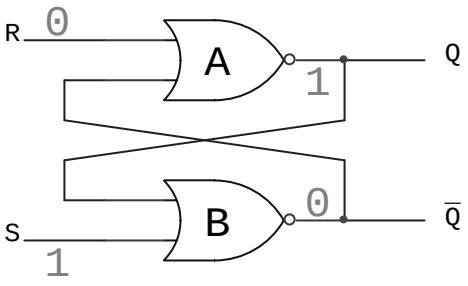
Initial Q=0, /Q=1
• Q and /Q must be different values. • When R is set to 1 • Gate A has a 1,0 input, therefore output Q=0, • Gate B has a 0,0 input, therefore output /Q=1

Initial Q=1, /Q=0
• Q and /Q must be different values. • When R is set to 1 • Gate A has a 1,1 input, therefore output Q=0, • Gate B has a 0,0 input, therefore output /Q=1

3.1.2 Set Condition



Q = 0, /Q = 1



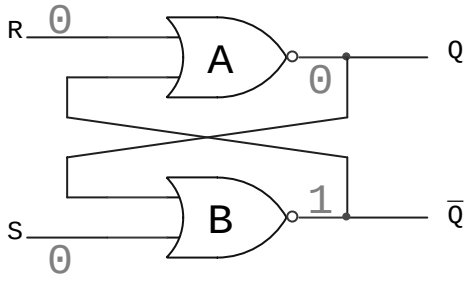
Q = 1, /Q = 0

Analysis:

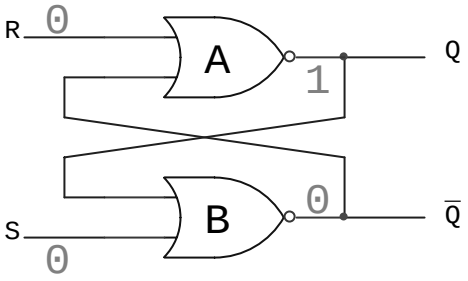
Initial Q=0, /Q=1
• Q and /Q must be different values. • When S is set to 1 • Gate B has a 1,0 input, therefore output /Q=0, • Gate A has a 0,0 input, therefore output Q=1

Initial Q=1, /Q=0
• Q and /Q must be different values. • When S is set to 1 • Gate B has a 1,1 input, therefore output /Q=0, • Gate A has a 0,0 input, therefore output Q=1

3.1.3 Hold Condition



Q = 0, /Q = 1



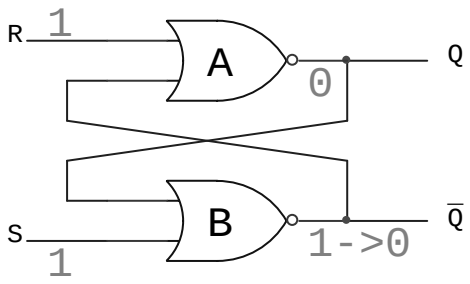
Q = 1, /Q = 0

Analysis:

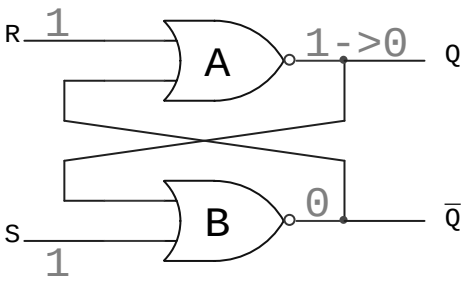
Initial Q=0, /Q=1
• Q and /Q must be different values. • When R is set to 1 • Gate A has a 0,1 input, therefore output Q=0, • Gate B has a 0,0 input, therefore output /Q=1

Initial Q=1, /Q=0
• Q and /Q must be different values. • When R is set to 1 • Gate A has a 0,0 input, therefore output Q=1 • Gate B has a 1,0 input, therefore output /Q=0

3.1.4 Disallowed Condition



Q = 0, /Q = 1



Q = 1, /Q = 0

Analysis:

Initial Q=0, /Q=1
• Q and /Q must be different values. • When R is set to 1, S is set to 1 • Gate A has a 1,0 input, therefore output Q=0 • Gate B has a 0,1 input, therefore output /Q=0

Initial Q=1, /Q=0
• Q and /Q must be different values. • When R is set to 1, S is set to 1 • Gate A has a 1,0 input, therefore output Q=0 • Gate B has a 0,1 input, therefore output /Q=0

ALARM BELLS SHOULD BE RINGING.

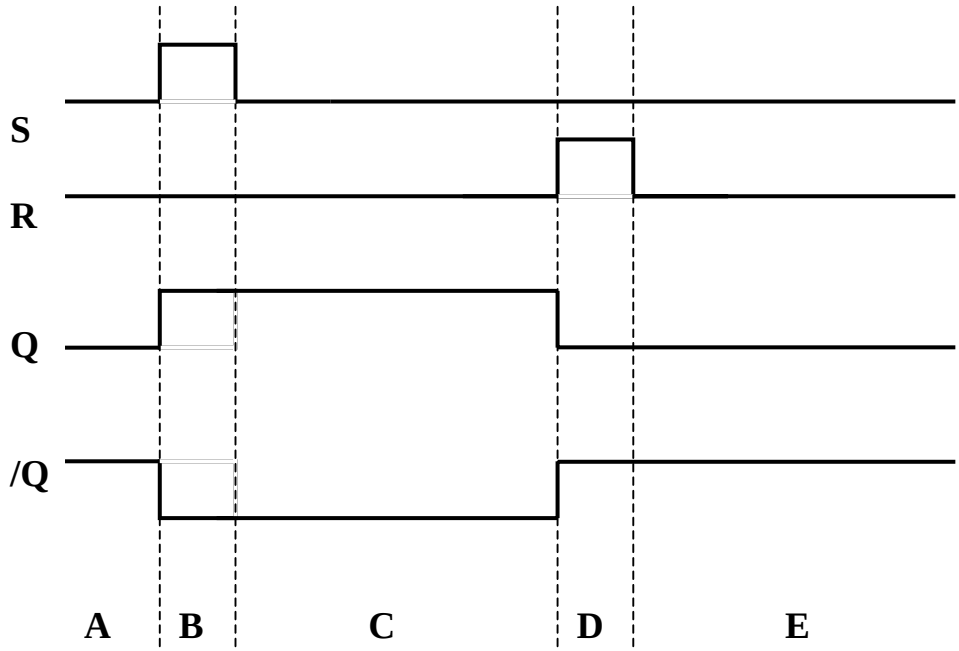
This ***violates*** our logic rules.
Q and NOT Q cannot both be 0.
Therefore R=1, S=1 cannot not be allowed to happen.
We avoid these inputs at all costs.

3.1.5 Truth Table for Set – Reset Latch

S	R	Q	/Q	Comment
1	0	1	0	Sets latch to 1
0	1	0	1	Resets latch to 0
0	0	hold	hold	Retains Q & /Q values
1	1	-	-	Disallowed

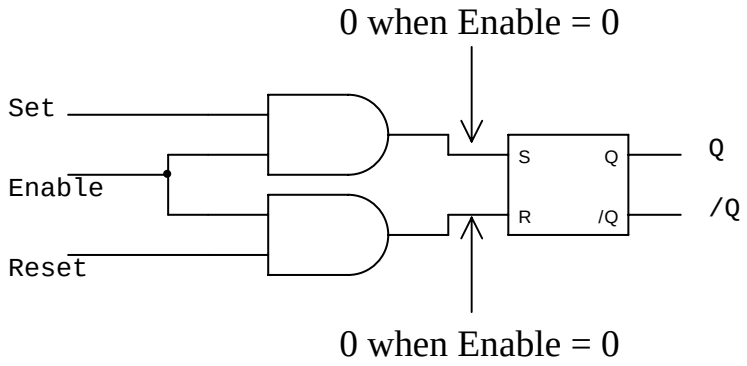
Timing Diagram

Initial Q=0, then a momentary *Set* Pulse, then a momentary *Reset* Pulse



Region	S	R	Description	Q
A	0	0	Hold	0
B	1	0	Set Latch	1
C	0	0	Hold previous	1
D	0	1	Reset Latch	0
E	0	0	Hold previous	0

3.2 Gated RS Latch



The AND gates are used to pass the Set and Reset signals to the latch when the Enable line is asserted.

The latch will operate normally when the Enable is HIGH.

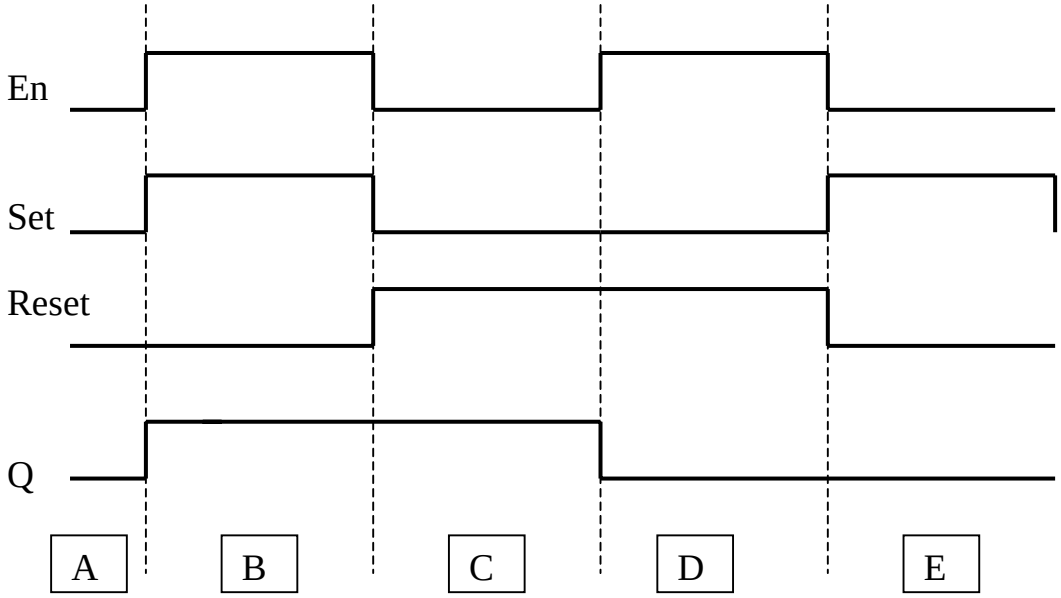
The latch will not respond when the Enable is LOW.

The following truth table for the gated SR latch can be constructed using the following properties of AND gates

X . 0 = 0
X . 1 = X

Enable	Set	Reset	S (Set . Enable)	R (Reset . Enable)	Result
0	0	0	0	0	No change
0	1	0	0	0	No change
0	0	1	0	0	No change
1	0	0	0	0	No change
1	1	0	1	0	Q=1
1	0	1	0	1	Q=0
1	1	1	1	1	Disallowed

Timing Diagram

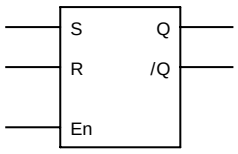


Region	En	Set	Reset	S	R	Description	Q
A	0	0	0	0	0	Unchanged	0
B	1	1	0	1	0	Set Latch	1
C	0	0	1	0	0	Unchanged	1
D	1	0	1	0	1	Reset Latch	0
E	0	1	0	1	0	Unchanged	0

Regions B & D, set and reset the latch since Enable is HIGH.

Regions A & C & E, do nothing since Enable is LOW.

Symbol



S is the *Set*.
R is the *Reset*.
En is the *Enable* (Gate).
Q is the *output*.

3.2.1 Integrated Circuit RS Latch (74279)

This contains 4 low active RS latches.

This is called the Quad Set-Reset Latch

Each latch has a R and S input, with only the Q output.

It should be noted that the R and S lines are low active.

Two of the latches are unusual in that they have 2 set lines. For most applications it is best to tie these lines together.

This device is **NOT** gated.

3.3 Gated D Latch

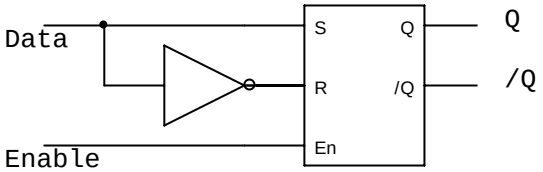
A D latch stands for Data Latch.

A D latch uses only one input to set and reset the latch.

This is achieved by placing a NOT gate between the S and R inputs of a gated SR latch.

The NOT guarantees that the unwanted R=S=1 does not occur.

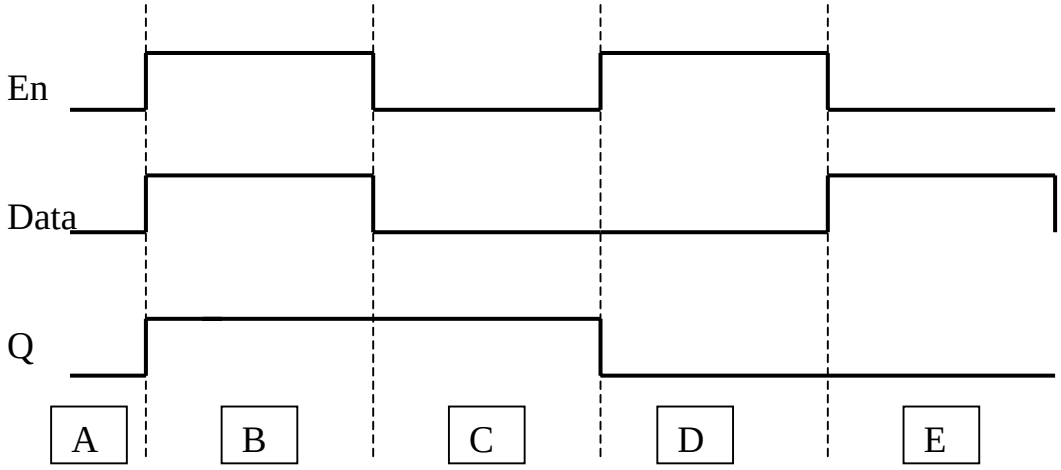
The enable controls the latching of the data.



Truth Table

Enable	Data	Result
0	0	No change
0	1	No change
1	0	Q=0
1	1	Q=1

Timing Diagram

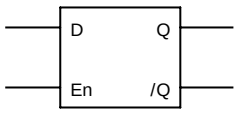


Region	En	Data	Description	Q
A	0	0	Unchanged	0
B	1	1	Load Data	1
C	0	1	Unchanged	1
D	1	0	Load Data	0
E	0	1	Unchanged	0

The data is loaded into the latch in regions B & D since Enable is HIGH.

Regions A & C & E, do nothing since Enable is LOW.

Symbol



D is the *Data*.
En is the *Enable* (Gate).
Q is the *output*.

3.3.1 Integrated Circuit D Latch (7475)

This contains 4 D latches.

It is called the 4-bit bistable latch.

Latches 0,1 share the same enable.

Latches 2,3 share the same enable.

Information present at a dat input (D) is transferred to the Q output when the enable is HIGH and the Q output will follow the D input as long as the enable is HIGH.

There are Q and /Q outputs for all the latches.

3.4 Triggering & Clocking

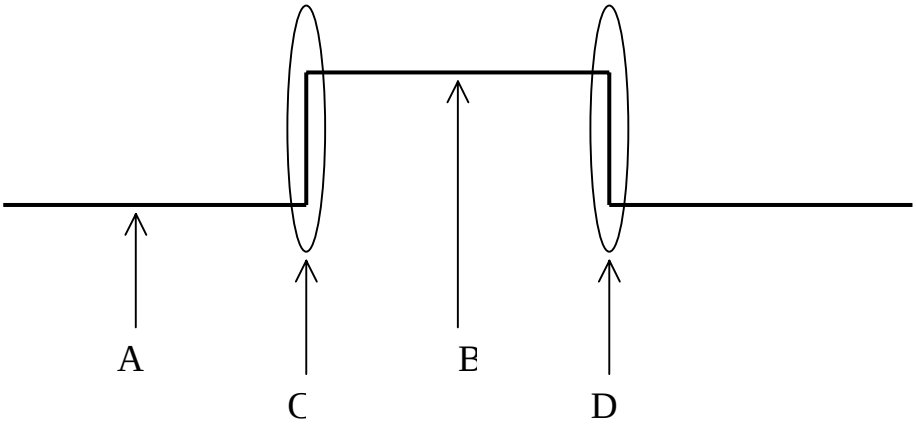
A trigger is a control signal used to initiate an action.

In the gated latches, the trigger is the enable line. Setting the enable HIGH allows the latch to be set or reset.

Triggers can be of two forms

1. Level Triggers (HIGH or LOW levels)
2. Edge Triggers (+ve or –ve going transitions)

Examining a pulse, indicates all the possible levels and edges



Letter	Comment
A	LOW level
B	HIGH level
C	Positive Edge (LOW -> HIGH Transition)
D	Negative Edge (HIGH -> LOW Transition)

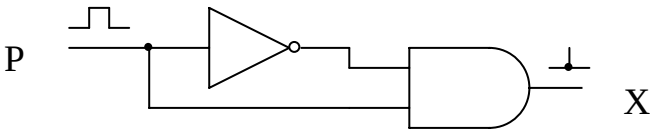
A *level trigger* means that an action is initiated on either a LOW or HIGH level.

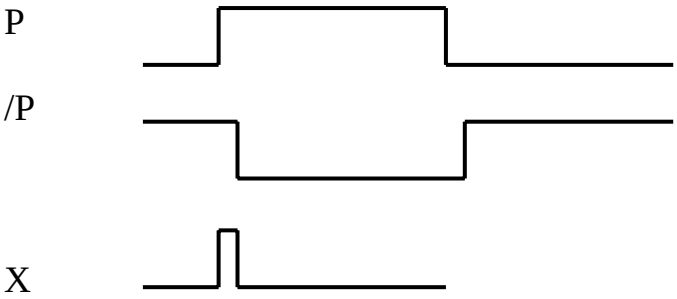
An *edge trigger* means that an action is initiated on either a positive or negative transition.

A *clock* is a series of pulses (Square Waves) used to synchronise actions. Generally the triggers are taken from the edges of the clock.

3.4.1 Edge Triggering

The positive edge triggering circuit is given below



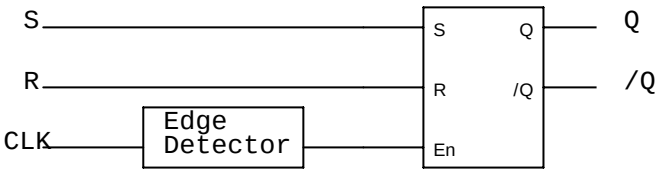


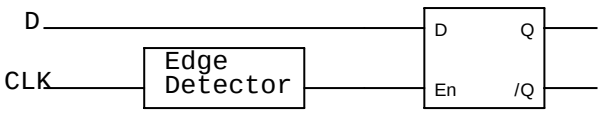
The propagation delay of the inverter causes a delay of a few nanoseconds between P and /P. The AND gate translates this into a narrow pulse (X) of the order of a few nanoseconds in duration.

Pulse X is long enough to trigger a change in the state of the latches.

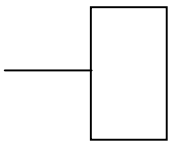
Q. How do you make a negative edge detector?
A. Invert the pulse P before applying to the circuit above.

Q. How do you make an edge triggered SR latch or D latch?
A. Add the edge detector to the enable line.

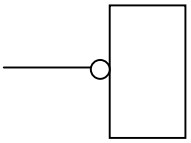




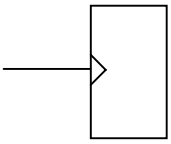
3.4.2 Symbols



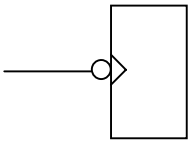
Positive Level Triggered



Negative Level Triggered



Positive Edge Triggered



Negative Edge Triggered

3.4.3 Truth Table

Positive Edge Triggered RS Flip-Flop

Edge	Set	Reset	Result
X	0	0	No change
↑	0	0	No change
↑	1	0	Q=1
↑	0	1	Q=0
↑	1	1	Invalid

Note:

X is don't care. (Can be either 0 or 1)

↑ indicates a LOW to HIGH (positive) transition.

Positive Edge Triggered D Flip-Flop

Edge	Data	Result
X	X	No change
↑	0	Q=0
↑	1	Q=1

Note:

X is don't care. (Can be either 0 or 1)

↑ indicates a LOW to HIGH (positive) transition.

3.4.4 Integrated Circuit D Flip-Flop (7474)

This contains 2 D-type flip-flops.

This is called the Dual D-Type Positive Edge-Triggered Flip-Flop.

There is an asynchronous preset and clear for these flip-flops to allow the initial state to be set.

There is a CP (clock pulse) input which requires the synchronising clock signal.

Information at the input is transferred to the outputs on the positive edge of the clock pulse. After the clock pulse input threshold has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the clock pulse input.

3.4.5 Integrated Circuit Octal D Latch (74273)

This is called an 8-bit Register.

This contains 8 x D latches which is ideal for computer applications.

Each latch contains 1 bit and 8 bits make one byte.

All 8 latches are controlled by a common clock signal.

Data is latched in on the positive edge of the clock.

All 8 latches can be simultaneously reset (cleared) by asserting the Master Reset (/MR) line.

This is a high-speed 8 bit register, consisting of 8 D-type flip-flops with a common clock and an asynchronous active LOW Master Reset.

3.5 Edge Triggered JK Flip-Flop

The JK is a widely used flip-flop.

J & K do not mean anything special.

The J is equivalent to a *set*.

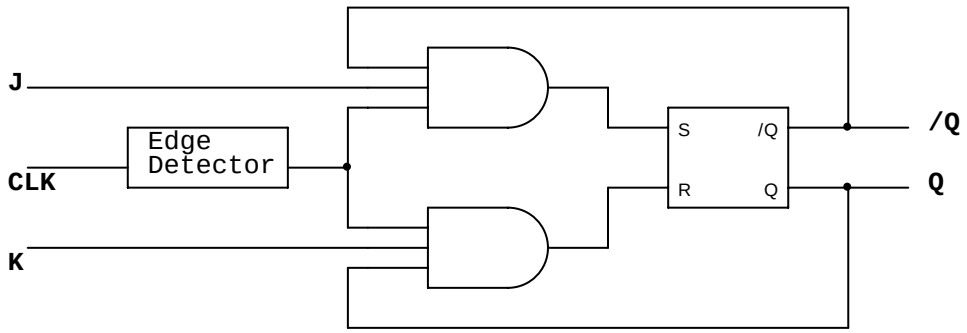
The K is equivalent to a *reset*.

A JK flip-flop acts like a RS flip-flop except that it does not have a invalid state.

The R=S=1 state has been replaced with a *toggle* state.

Toggle means that the output (Q) will change to the opposite state (0 to 1 or 1 to 0) after every clock transition.

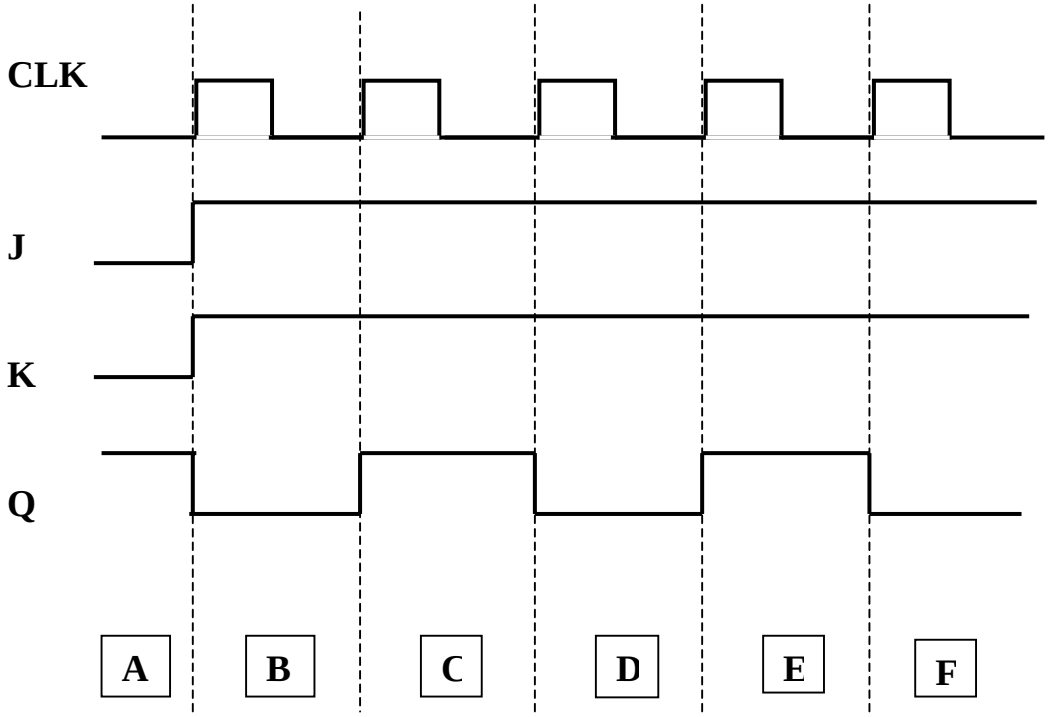
The JK is an RS flip-flop with feed back from Q and /Q.



Truth Table

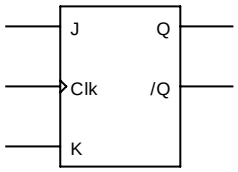
CLK	J	K	Result
X	0	0	No change
↑	0	0	No change
↑	1	0	Q=1
↑	0	1	Q=0
↑	1	1	Toggle

3.5.1 Illustration of Toggle



Region	En	J	K	Description	Q
A	0	0	0	Initial	1
B	↑	1	1	Toggle	0
C	↑	1	1	Toggle	1
D	↑	1	1	Toggle	0
E	↑	1	1	Toggle	1
F	↑	1	1	Toggle	0

Symbol



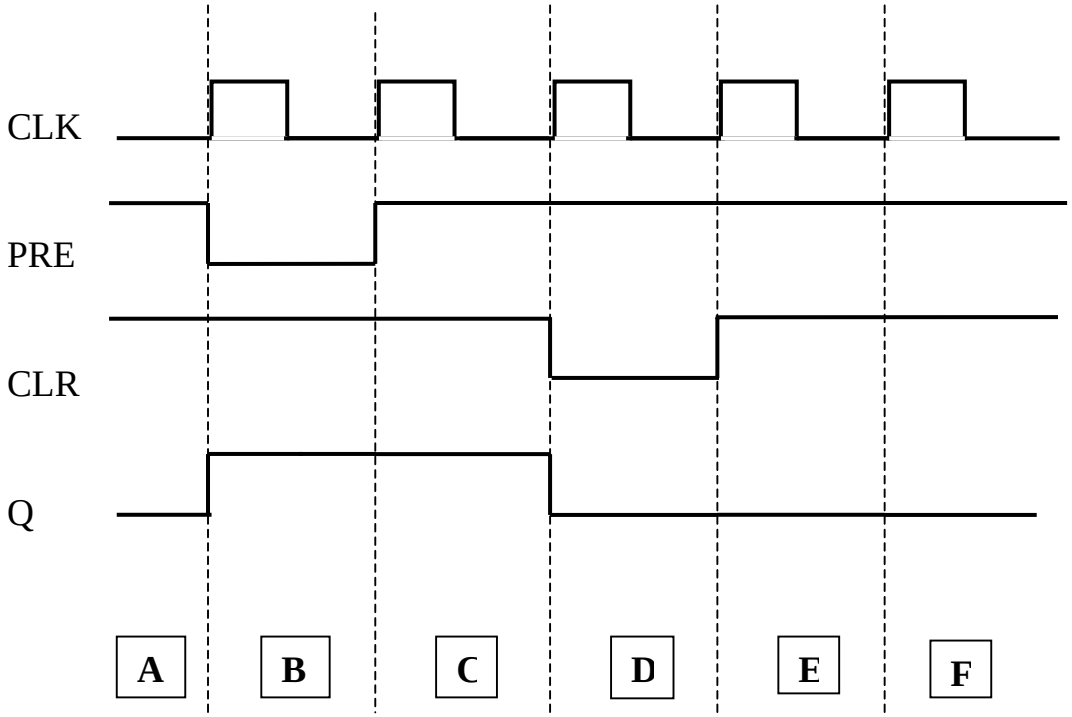
3.5.2 Asynchronous Preset and Clear Inputs

The previous flip-flops are synchronous because data is transferred to the flip-flops output on the clock signal.

Asynchronous inputs change the state of the flip-flop without requiring a clock pulse.

The asynchronous inputs are normally *preset* and *clear*, which allows the flip-flop to be set and reset.

The preset and clear are level triggered, generally LOW active.

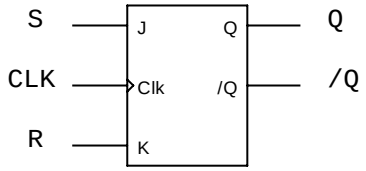


3.5.3 Other types of flip-flops from JK Flip-Flops

JK flip-flops are widely used because of their versatility. They can be easily adapted for use as a RS flip-flop, D flip-flop, and T flip-flop.

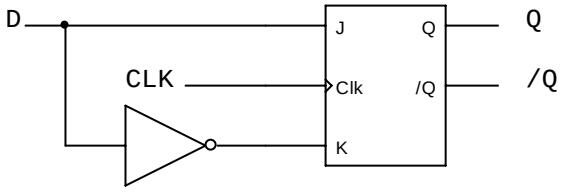
Edge Triggered RS flip-flop

The RS flip-flop can be constructed out of a JK flip-flop by setting S=J and R=K.



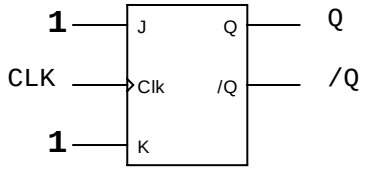
Edge Triggered D flip-flop

A D flip-flop can be constructed out of a JK flip-flop by connecting an inverter between J and K.



Edge Triggered T flip-flop

A Toggle flip-flop can be constructed out of a JK flip-flop by connecting J and K to HIGH.



3.5.4 Integrated Circuit JK Flip-Flop (7476)

This contains 2 JK-type flip-flops.

This is called the Dual JK Flip-Flop.

There is an asynchronous low active preset (/SD) and clear (/CD) for these flip-flops to allow the initial state to be set.

There is are 2 CP (clock pulse) inputs which synchronises the flip-flops to the clock.

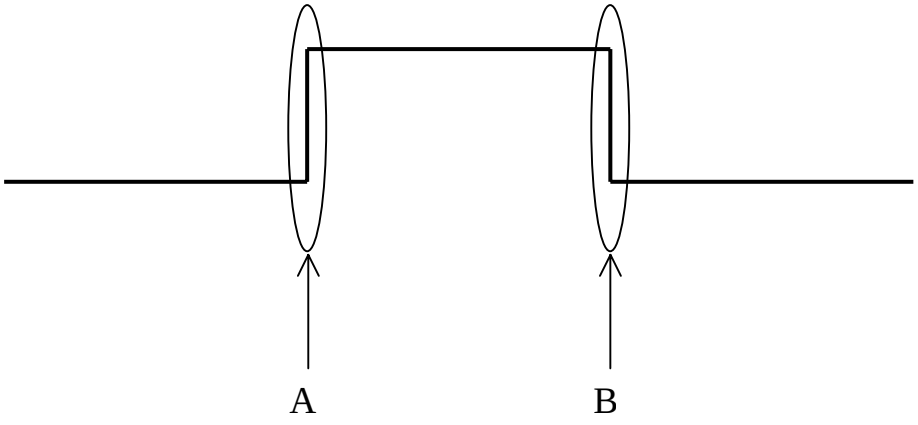
When the Clock Pulse input is HIGH, the JK inputs are enabled and data is accepted. This data will be transferred to the outputs according to the Truth Table on the HIGH-to-LOW clock transitions.

3.6 Master – Slave Flip-Flops

A master-slave flip-flop is a flip-flop that responds to a pulse rather than an edge or a level.

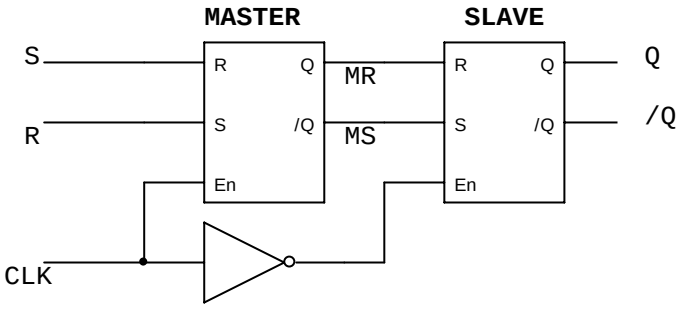
It consists of two flip-flops called the master and the slave.

The master flip-flop latches the inputs on the positive edge of the clock and transfers them to the slave on the negative edge of the clock.



Region	Description
A	Inputs gated into the Master
B	Master transfers inputs to Slave

Eg
RS Master Slave Flip-Flop



The Master latches the SR inputs on the positive edge of the clock.

The Slave latches the MR and MS inputs and generates the Q and /Q on the negative edge of the clock.

3.7 AC Characteristics

Propagation Delay Time (t_{PLH}, t_{PHL})

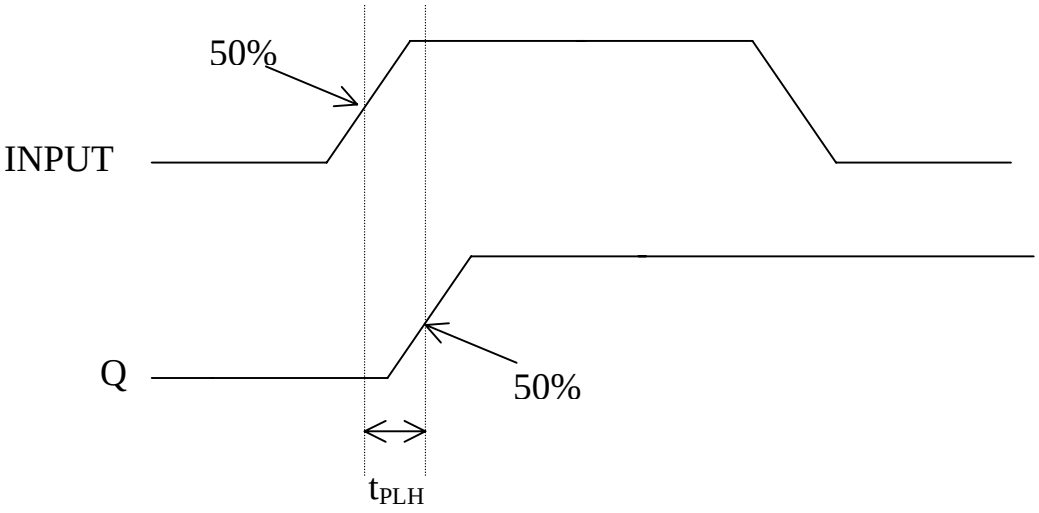
The time taken from the triggering input transition to the corresponding output transition.

The transitions are measured from the 50% point.

The output (Q) is measured relative to the:

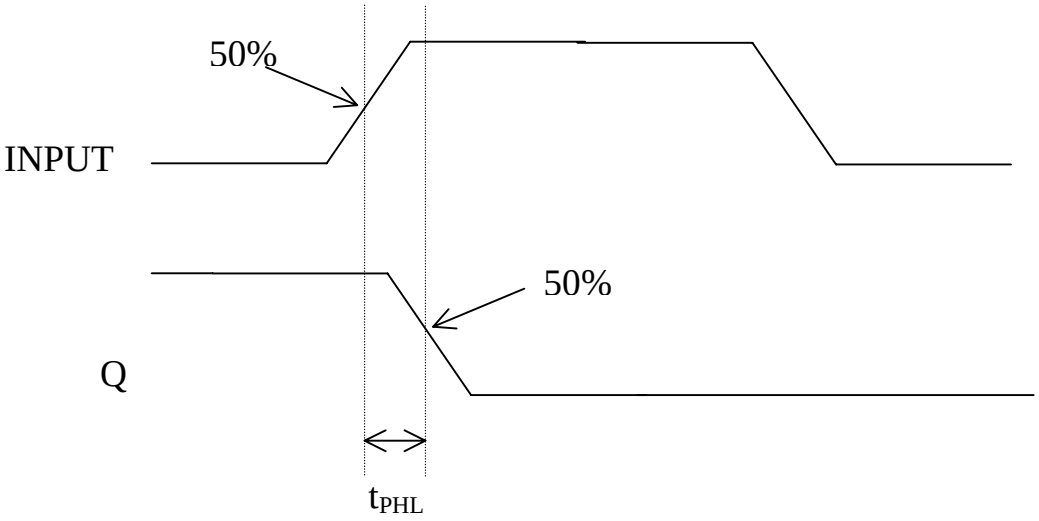
1. Clock Pulse input.
2. Preset and Clear inputs.

t_{PLH}



The input is either the *Clock* or the *Preset* inputs.

t_{PHL}

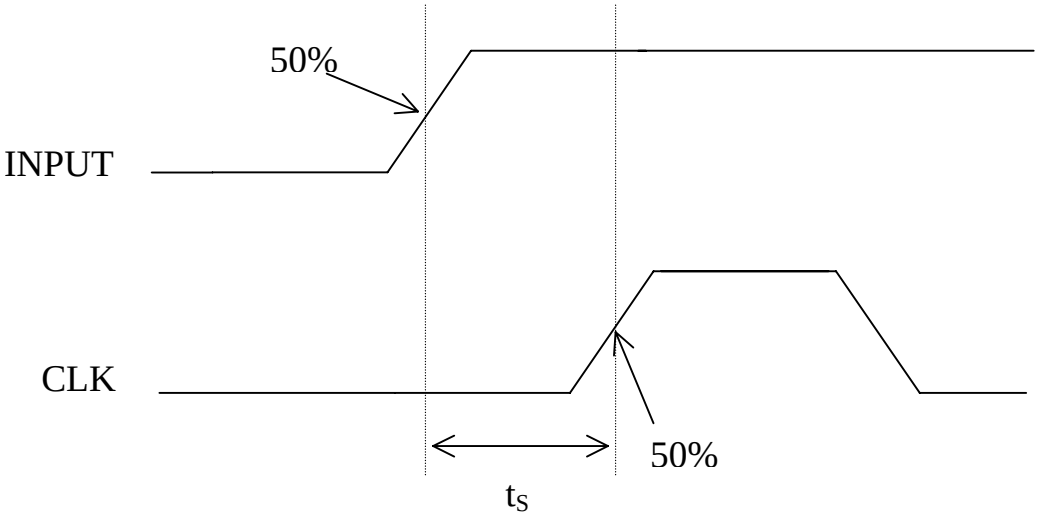


The input is either the *Clock* or the *Preset* inputs.

Set-up Time (t_s)

The minimum time that the logic levels must be maintained on the inputs prior to the clock transition.

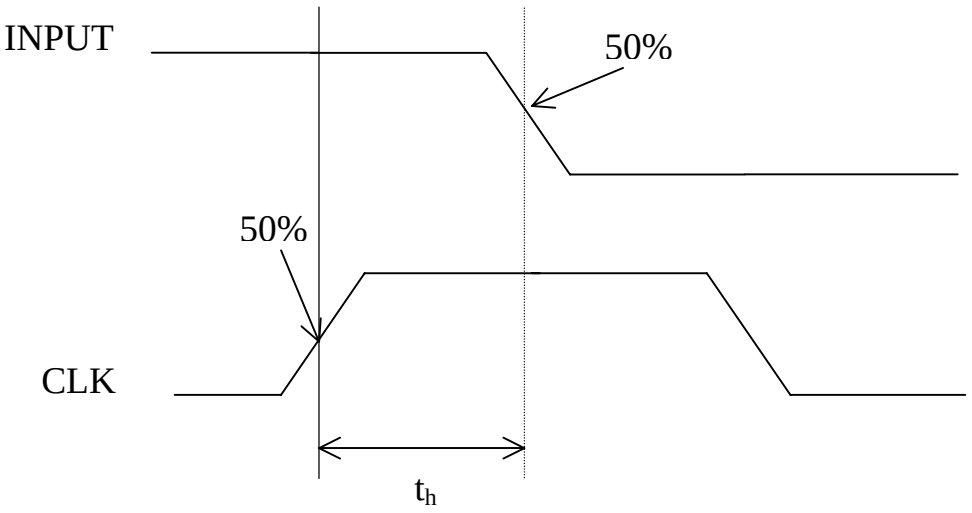
This guarantees that the inputs are reliably clocked into the flip-flop.



Hold Time (t_h)

The minimum time that the logic levels must be maintained on the inputs after the clock transition.

This guarantees that the inputs are reliably clocked into the flip-flop.



Maximum Clock Frequency (f_{max})

The highest frequency which can reliably be used as a clock.

Pulse Width (t_w)

The minimum pulse width for the preset, clear, and clock inputs.

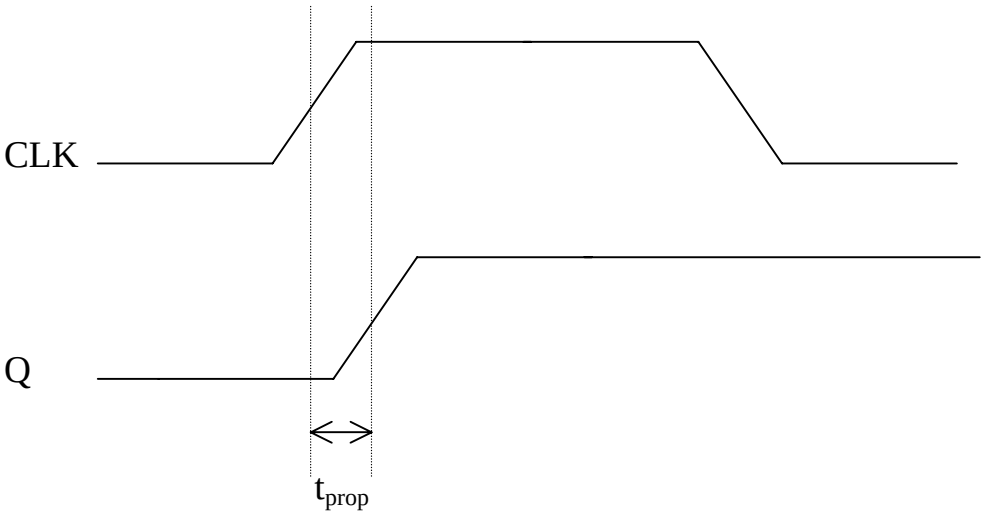
3.8 DC Characteristics

Power Dissipation

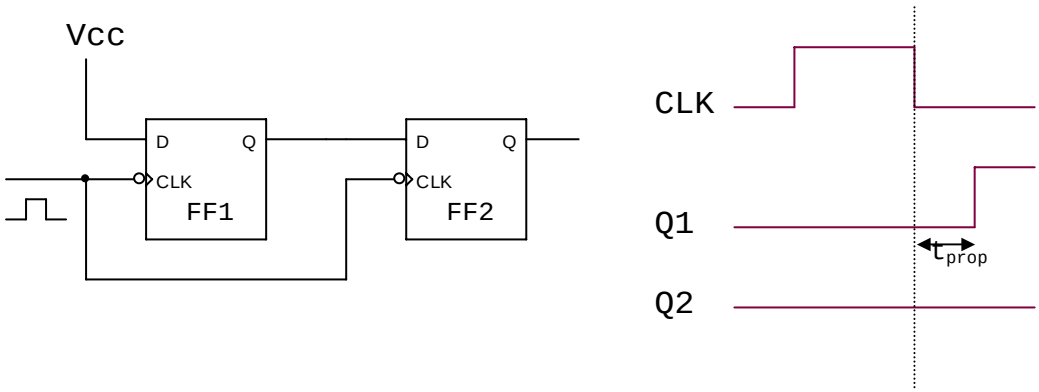
The total power consumption of the device.

3.9 Propagation Delay

Propagation delays can cause timing problems with flip-flop circuits. The propagation delay is the time taken for the flip-flop to respond after receiving the active clock edge.



The following circuit illustrates a potential timing problem with triggering flip-flops off the same clock pulse.



The idea is that when the negative edge of the clock pulse occurs, the output of FF1 is latched in FF2.

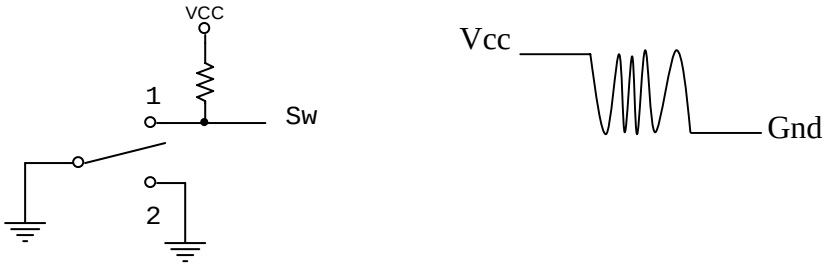
This will not happen as expected due to the propagation delay of the FF1. Instead FF2 will latch output of FF1 before FF1 has had time to change its output.

We use this effect to our advantage when we make ripple counters in module 3.

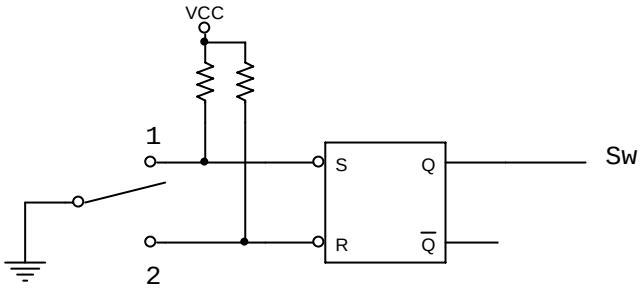
The way to fix the timing problem is to make FF1 latch the data on the positive edge and make FF2 latch the data on the negative edge.

3.10 RS Latch circuit to remove contact bounce

A switch circuit is shown below. It is expected that when the when the switch makes contact with pole 1 the line will go low. However, this is not the case. Switch bounce can cause the voltage to randomly fluctuate between Vcc and ground until it finally settles at ground. This can cause false triggering in digital circuits.



The contact bounce can be eliminated using an RS latch as in the following circuit.



When the switch is connected to pole 1, the *set* line is LOW and the *reset* line is HIGH. This sets the latch forcing Sw HIGH. When the switch is connected to pole 2, the *reset* line is LOW and the *set* line is HIGH. This resets the latch forcing Sw LOW. Contact bounce will not affect this circuit as long as the initial contact with pole 2 is long enough to assert the *reset*.