**Wasit University**
**Engineering Faculty**
**Electrical Eng. Depart.**

**Subject: Digital Techniques**
**Time: 3 Hour**
**Final Exam**

**2016 - 2017**

***Q1****/Design a full adder using two half adders and one OR Gate.* (**10 marks**)

***Q2****/Design 4 bit PISO.* (**10 marks**)

***Q3****/ Design a combinational circuit whose input is a 3-bit number and whose output is the 2's complement of the input number.* **(10 marks**)

***Q4****/Answer* ***ONE*** *branch only* **(10 marks**)

A. Design 8 to 1 Multiplexer from 4 to 1 multiplexes and 2 to 1 Multiplexer.
B. Design 1 to 4 Demultiplexer and show the truth table and equation & combinational circuit.

***Q5****/ A combinational circuit is defined by the following three Boolean functions*

(**10 marks**)

$$F_1(A,B,C) = \sum m(0,3,4)$$
$$F_2(A,B,C) = \sum m(1,2,7)$$
$$F_3(A,B,C) = \prod M(0,1,2,4)$$

*Implement the circuit with a decoder and external OR gates.*

***Q6****/*

*A-* Simplifying **THREE** of the following Boolean function using k-map (**12 marks**)

1. $F(W,X,Y,Z) = \sum m(0,1,2,4,5,6,8,9,12,13,14)$
2. $F = \bar{A}\bar{B}\bar{C} + \bar{B}C\bar{D} + A\bar{B}\bar{C} + \bar{A}BC\bar{D}$
3. $F = (\bar{A} + \bar{C}).(A + B + D).(A + \bar{B} + C).(\bar{A} + \bar{B} + \bar{D})$
4. $F(W,X,Y,Z) = \sum m(4,6,7,8,12,15), d(W,X,Y,Z) = \sum m(2,3,5,10,11,14)$

*B- Simplify the Boolean Function F and implemented it with NAND and NOR gates*

***(*8 mark)**

$$F = A\bar{C} + ACE + AC\overline{E} + \overline{A}C\overline{D} + \overline{A}\overline{D}\overline{E}$$