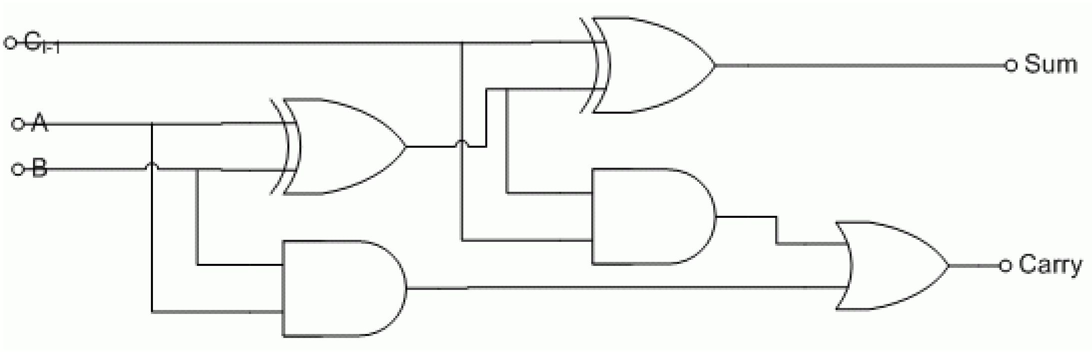
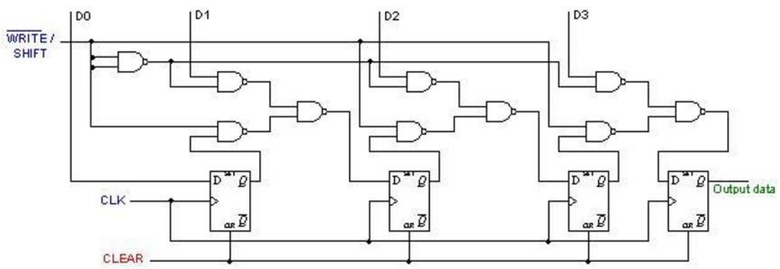
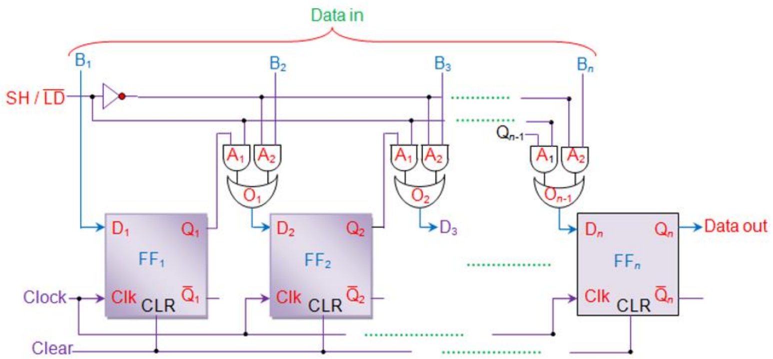
Q1*/Design a full adder using two half adders and one OR Gate.*

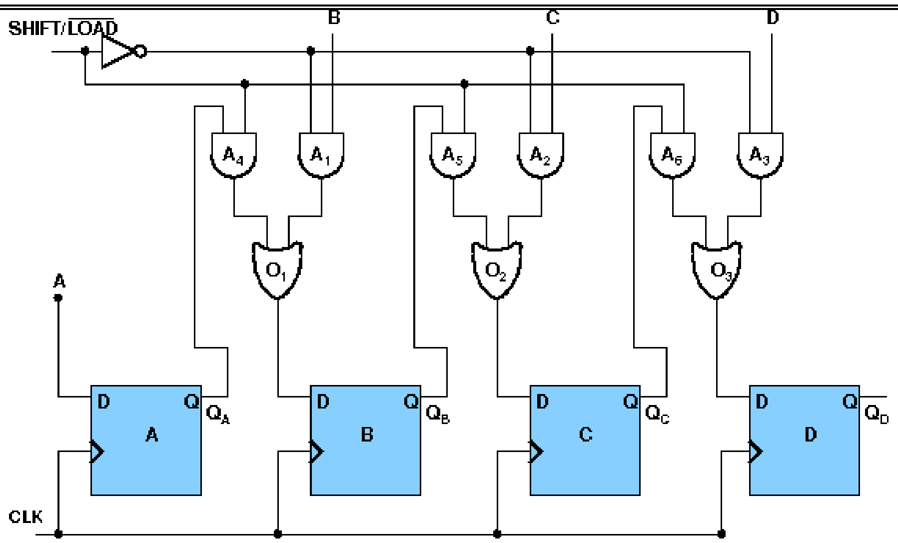


Q2*/Design 4 bit PISO.*

Drawing any one of follow is correct



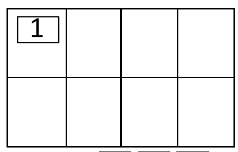




***Q3/** Design a combinational circuit whose input is a 3-bit number and whose output is the 2's complement of the input number.*

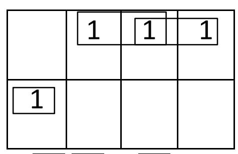
QA_1	A_2	A_3		F_1	F_2	F_3	F_4
0	0	0		1	0	0	0
0	0	1		0	1	1	1
0	1	0		0	1	1	0
0	1	1		0	1	0	1
1	0	0		0	1	0	0
1	0	1		0	0	1	1
1	1	0		0	0	1	0
1	1	1		0	0	0	1

F_1



$$F_1 = \overline{A_1}\,\overline{A_2}\,\overline{A_3}$$

F_2



$$F_2 = A_1\,\overline{A_2}\,\overline{A_3} + \overline{A_1}\,A_3 + \overline{A_1}\,A_2$$

F_3

	1		1
	1		1

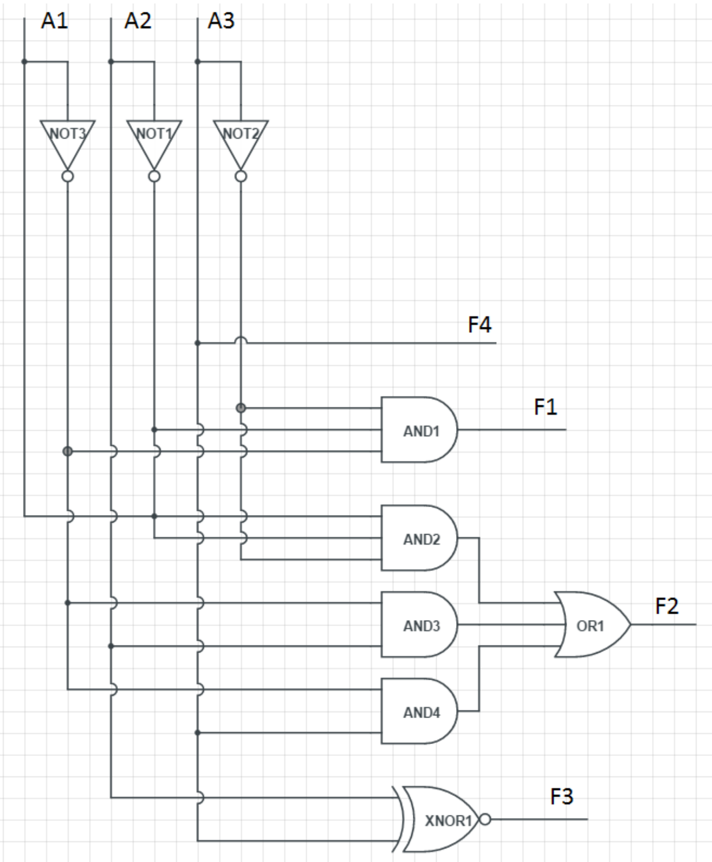
$$F_3 = \overline{A_2}A_3 + A_2\overline{A_3}$$

$$F_3 = A_2 \oplus A_3$$

F_4

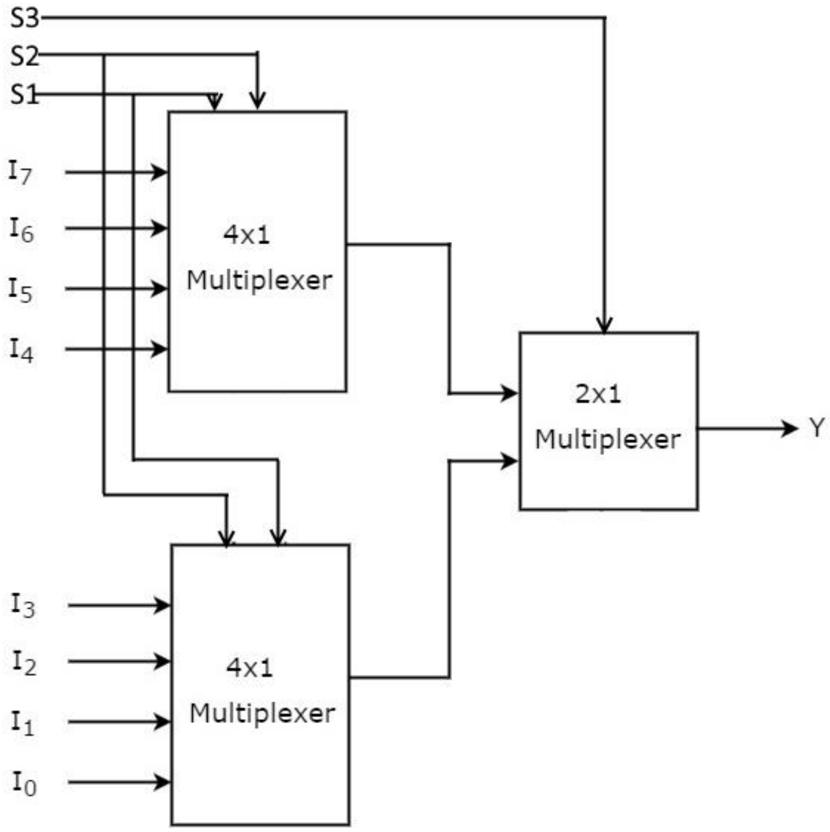
	1	1	
	1	1	

$$F_4 = A_3$$



__Q4__/Answer __ONE__ branch only

A. Design 8 to 1 Multiplexer from 4 to 1 multiplexes and 2 to 1 Multiplexer.

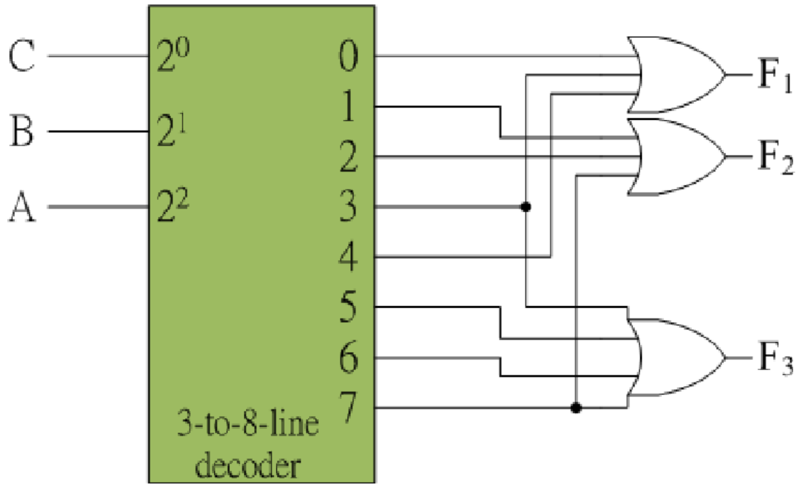


Q5/ *A combinational circuit is defined by the following three Boolean functions*

$$F_1(A,B,C) = \sum m(0,3,4)$$

$$F_2(A,B,C) = \sum m(1,2,7)$$
$$F_3(A,B,C) = \prod M(0,1,2,4)$$

Implement the circuit with a decoder and external OR gates.



Q6/

1. $F(W,X,Y,Z) = \sum m(0,1,2,4,5,6,8,9,12,13,14)$

1	1		1
1	1		1
1	1		1
1	1		

$F(w,x,y,z) = \bar{y} + \bar{w}\bar{z} + x\bar{z}$

2. $F = \bar{A}\bar{B}\bar{C} + \bar{B}C\bar{D} + A\bar{B}\bar{C} + \bar{A}BC\bar{D}$

1	1		1
			1
1	1		1

$F = \bar{B}\bar{C} + \bar{B}\bar{D} + \bar{A}C\bar{D}$

3. $F(W,X,Y,Z) = \sum m(4,6,7,8,12,15), d(W,X,Y,Z) = \sum m(2,3,5,10,11,14)$

		x	x
1	x	1	1
1		1	x
1		x	x

$$F(w,x,y,z) = y + x\bar{z} + w\bar{z}$$

$$F(w,x,y,z) = y + \bar{w}x + w\bar{z}$$

B- Simplify the Boolean Function F and implemented it with NAND and NOR gates

$$F = A\bar{C} + ACE + AC\bar{E} + \bar{A}C\bar{D} + \bar{A}\bar{D}\bar{E}$$